AMENDMENTS TO THE CLAIMS:

Please amend claims as follows:

1. (currently amended) An arrangement for testing an integrated circuit, the arrangement comprising a data word generator which supplies deterministic data words, means for test pattern generation having one or more bit flipping logic circuits and at least one bit flipping controller~~, which~~ to modify the deterministic data words such that prescribed, deterministic test patterns which can be fed to inputs of the integrated circuit to be tested, are produced, and having comparison means for comparing test output patterns of the integrated circuit with at least one desired output pattern, the arrangement being provided outside the integrated circuit to be tested.

2. (previously presented) The arrangement as claimed in claim 1, wherein a feedback shift register is provided as the data word generator.

3. (currently amended) The arrangement as claimed in claim 1, wherein ~~provided as means for test pattern generation is a~~ the at least one bit flipping controller ~~which~~ controls and/or drives the bit flipping logic circuits such that the deterministic data words are modified in a bitwise fashion such that the prescribed, deterministic test patterns are produced.

4. (currently amended) The arrangement as claimed in claim 1, wherein there is provided a masking logic circuit ~~the effect of which~~

~~is~~ arranged so that the comparison means exclusively compare prescribed test output patterns of the integrated circuit to be tested with the desired output patterns.

5. (currently amended) The arrangement as claimed in claim 3, wherein a test pattern counter is provided which counts a clock signal and supplies the counting result to the bit flipping controller and/or ~~the~~ a masking logic circuit.

6. (currently amended) ~~The arrangement as claimed in claim 1, wherein~~ An arrangement for testing an integrated circuit, the arrangement comprising a data word generator which supplies deterministic data words, means for test pattern generation, which modify the deterministic data words such that prescribed, deterministic test patterns which can be fed to inputs of the integrated circuit to be tested, are produced, comparison means for comparing test output patterns of the integrated circuit with at least one desired output pattern, the arrangement being provided outside the integrated circuit to be tested, and having a signature register ~~is provided~~ which logically intercombines consecutive test output patterns, and whose final combination result is compared with a desired output pattern.

7. (previously presented) The arrangement as claimed in claim 1, wherein the desired output pattern is generated by means of the data word generator and the means for test pattern generation.

8. (previously presented) The arrangement as claimed in claim 1, wherein the arrangement is implemented as a programmable logic circuit.

9. (previously presented) The arrangement as claimed in claim 1, wherein the arrangement is provided on a test board which is connected between a test system and the integrated circuit to be tested.

10. (currently amended) A method for testing an integrated circuit, in which method deterministic data words are modified via bit flipping logic circuits and at least one bit flipping controller ~~such~~ so that prescribed, deterministic test patterns are produced which can be fed to inputs of the integrated circuit to be tested, test output patterns of the integrated circuit to be tested being compared with at least one desired output pattern, and the method being carried out outside the integrated circuit to be tested.